



# Chiplets – The New Frontier of Electronic Design

Challenges and Solutions in Chiplet-based Designs

Moshe Zalcborg



# Nice to meet you!

Veriest

Moshe Zalcborg

Presently:

- CEO at Veriest Solutions
- Partner at Silicon Catalyst

Veriest



Formerly:

- GM Israel at Cadence Design System
- VP BizDev at Presto Engineering

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PRESTO  
Engineering



Semiconductor Engineering Consultancy company, founded in 2007



Headquartered in Israel, 5 additional sites in Europe: UK, Hungary, Serbia



Customers in US, Europe, Israel



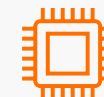
Full flow solution provider



Software



Front-end  
(Design & Verification)



Back-end  
(DFT & Physical Design)

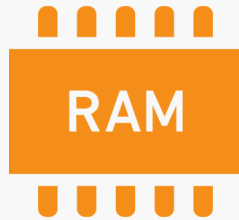
# We have a unique vantage point!



# Monolithic SoCs – key limiting factors



Geometry Scaling



Local Memory

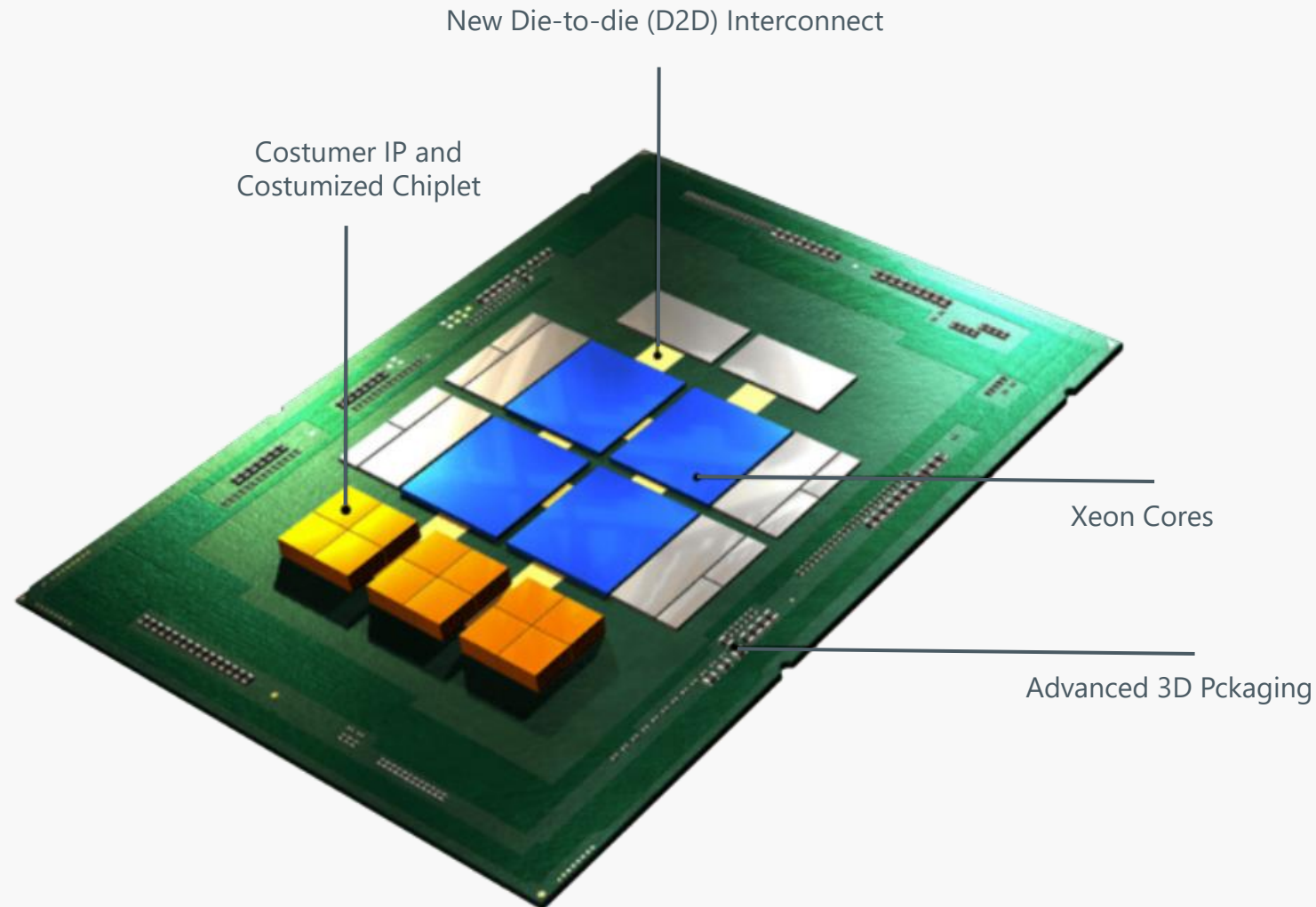


I/O bandwidth



Economics

# Multi-die solutions/ chiplets



# Chiplets - Key benefits



**Functionality  
Scale-up**



**Reduced  
development costs**



**Rapid  
creation of variants**



**Shorter  
time to market**



**More resilient  
supply chain**



**Lower risk**



**Power/performance**



**Reliability**

# Chipllets in the news

≡ Forbes

AI

The Chiplet's Time Is Coming, It's Here, Or Not.

DESIGNLINES | SOC DESIGNLINE

Are Chiplets Enough to Save Moore's Law?

EE Times

## Automotive Relationships Shifting With Chiplets

116  
Shares



16



14



SEMICONDUCTOR ENGINEERING  
DEEP INSIGHTS FOR THE TECH INDUSTRY

What Are Chiplets and Why They Are So Important for the Future of Processors

TECHSPOT



# It's even a Geopolitical issue!

*U.S. Focuses on Invigorating 'Chiplet' to Stay Cutting-Edge in Tech*  
**The New York Times**

**€16m project to secure the  
chiplet supply chain in  
Europe**

Business news | September 20, 2022

By Nick Flaherty



**Chinese chiplet  
architecture for data  
centres, automotive**

Business news | March 31, 2023

By Nick Flaherty



**Japan keen on building chiplet technology and  
ecosystem**

Chiang, Jen-Chieh, Taipei; Willis Ke, DIGITIMES  
Asia

| ⌚ Monday 17 April 2023 |



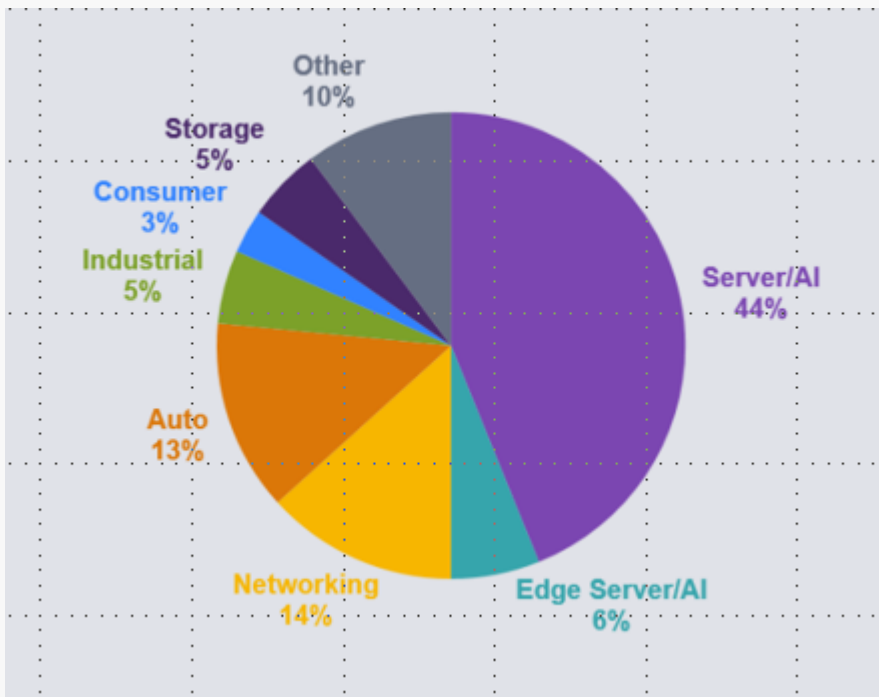
**DIGITIMES  
asia**



# It's happening now!

Veriest

Synopsys is tracking >100 multi-die designs



Source: Synopsys

Semi's



Systems



Startups



# There are major technical challenges:



System architecture &  
partition



Software development &  
modelling



System verification –  
coverage & capacity



Design flows  
& methodologies



Safety & Security  
considerations



Die-to-die  
connectivity



Signal integrity  
& signoff



Test &  
manufacturability

**Let's get started!**

# Our Agenda

1. **"Chiptlets are Enablers of Compute Expansion to Next Level"**  
François Piednôel, Distinguished Chief mSoC Architect at Mercedes-Benz
2. **"Chiptlets Interfaces and Interoperability"**  
Igor Elkanovich, CTO at GUC
3. **"Design methodologies and flows to lower the barrier to chiptletization"**  
Andreas Olofsson, CEO, Zero ASIC
4. **"UCle simulation specialist"**  
Anunay Bajaj, Cadence Design Systems, Inc.



# Chiplets are Enablers of Compute Expansion to Next Level

*François Piednöel, Distinguished Chief mSoC Architect at Mercedes-Benz*



# Chipelets Interfaces and Interoperability

*Igor Elkanovich, CTO at GUC (Global Unichip)*



# Design methodologies and flows to lower the barrier to chipletization

*Andreas Olofsson, CEO, Zero ASIC*





# Verification of chiplet-based designs: Challenges and solutions

*Anunay Bajaj, Cadence Design Systems, Inc.*





# Thank you!

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